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Evaluation of the Delamination in a Flip Chip Using Anisotropic Conductive Adhesive Films Under Moisture/Reflow Sensitivity Test

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***Abstract*—Anisotropic conductive adhesive films (ACFs) have been used for electronic assemblies such as the connection between a liquid crystal display panel and a flexible printed circuit board. ACF interconnection is expected to be a key technology for flip chip packaging, system-in-packaging, and chip size packaging. This paper presents a methodology for quantitative evaluation of the delamination in a flip chip interconnected by an ACF under moisture/reflow sensitivity tests. Moisture concentration after moisture absorption was obtained by the finite element method. Then, the vapor pressure in the flip chip during solder reflow process was estimated. Finally the delamination was predicted by comparing the stress intensity factor of an interface crack due to vapor pressure with the delamination toughness. It is found that the delamination is well predicted by the present methodology.**

***Index Terms*—Anisotropic conductive adhesive films (ACFs), delamination toughness, flip chip, moisture/reflow sensitivity test, reliability, stress intensity factor.**

I. Introduction

An anisotropic conductive adhesive film (ACF) is an adhesive containing conductive particles that supply electrical interconnections. Most of the current products are thermoset plastics. The ACF has been used for electronic assemblies such as the connection between a liquid crystal display (LCD) panel and a flexible printed circuit board (PCB) [1], [2]. Compared with traditional solder interconnection technology, the ACF interconnections have several advantages such as fine pitch, flexibility, low temperature processing, etc. The ACF interconnection is expected to be a key technology for flip chip packaging, system-in-packaging, and chip size packaging (CSP) [3]–[8].

Flip chip packages interconnected by the ACF are often used, together with surface mount devices (SMDs). In such a case, solder interconnections are utilized for the SMDs, so the ACFs in the flip chip packages are subjected to temperatures ranging from 240 °C to 245 °C during the solder reflow process. In addition to an increase in electric resistance, electric disconnection is also sometimes observed in the flip chip packages using the ACF interconnections during the solder reflow process [9], [10]. Such phenomena are caused by the delamination initiated from the interface between a chip and the ACF or a substrate and the ACF. It is therefore important to ensure the mechanical reliability of the ACF interconnections when they are used for flip chip packages instead of solder interconnections.

In the present paper, a methodology for evaluating the delamination of the ACF interconnection is proposed. Many researchers have previously studied to predict crack occurrence from a corner of jointed components in plastic packages [11]–[14]. In these studies, fracture mechanics were applied to the failure of plastic packages. As in these studies, we applied the fracture mechanics for an interface crack to the delamination of the ACF interconnection. The delamination tests are performed on joints composed of the ACF and the constituent materials of a flip chip. Then the delamination strengths are evaluated using the stress intensity factors of an interface crack between jointed dissimilar materials. The moisture concentration in the flip chip after a moisture absorption test is analyzed by the finite element method, and the vapor pressure caused by the solder reflow process was estimated. Finally the delamination in the flip chip during the solder reflow process was predicted by comparing the delamination strength with the stress intensity factors caused by vapor pressure.

II. Estimation of Delamination Strength

A. Delamination Tests

Delamination tests were performed on opening delamination specimens, lap joint specimens, and three-point bending specimens, as shown in Fig. 1. The initial delamination was introduced by a painting release agent on the surface of a silicon chip, on the surface of a substrate, or on the surface of an aluminum plate. Since the silicon chip is very brittle, the chip was reinforced by pasting a substrate (a lap joint specimen and a three-point bending specimen) or a support plate (an opening delamination test specimen) using epoxy adhesive resin to prevent its failure due to bending force. Delamination tests were performed at five different temperatures, 25 °C, 60 °C, 95 °C, 120 °C , and 240 °C, and at the test speed of 1 mm/min. The opening test was performed using a special apparatus as shown in Fig. 2. In this figure, the support plate has two roles, as a reinforced plate and as the location where the specimen is attached

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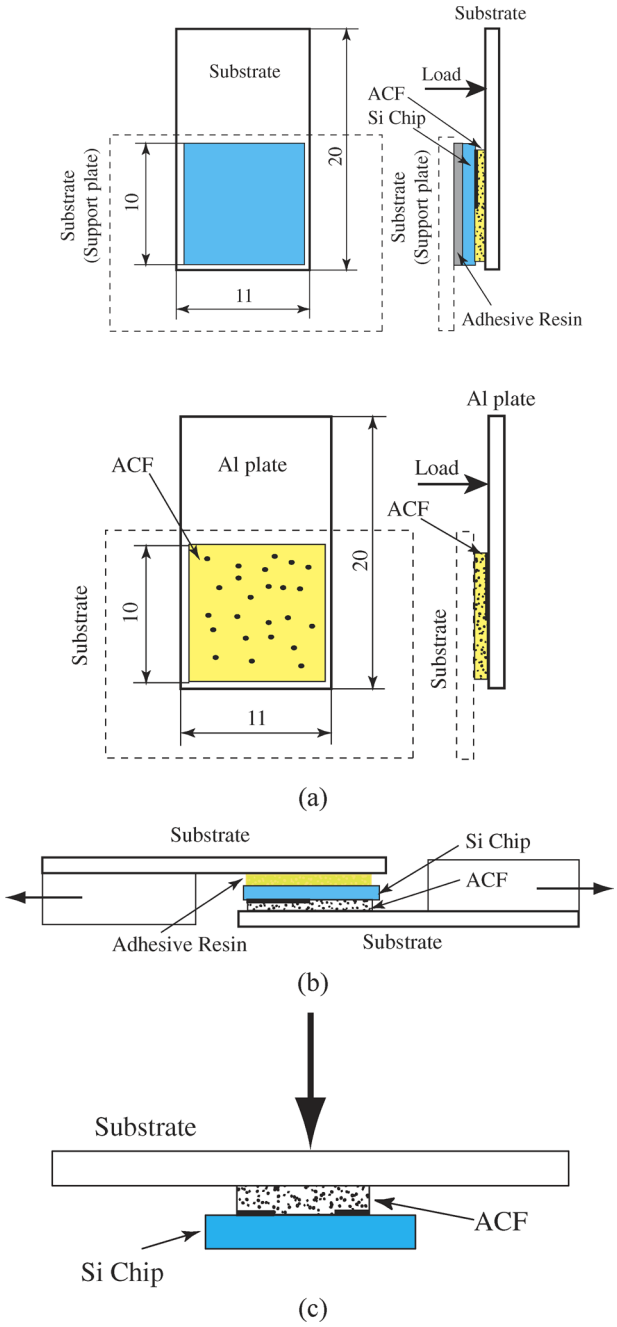


Fig. 1. Schematic of delamination test specimens. (a) Opening delamination specimen. (b) Lap joint specimen. (c) Three-point bending specimen.

to the testing machine. The lap joint test and the three-point bending tests were carried out using an Instron-type testing machine (Shimazu Autograph 5000E). In most cases, the load-displacement curve was straight. We obtained the delamination toughness as the maximum load. The delamination loads obtained from the tests were converted into the stress intensity factors of an interface crack between dissimilar materials, then used to represent the delamination toughness.

B. Stress Intensity Factors of an Interface Crack Between Dissimilar Materials

The delamination load obtained by the delamination test cannot be used as a measure for delamination strength, because

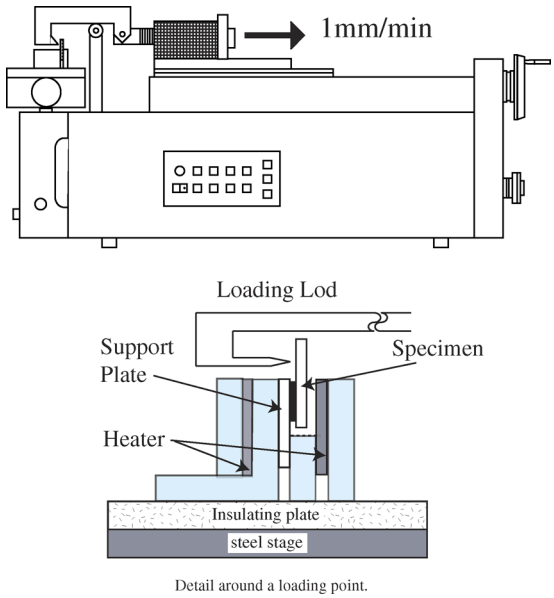


Fig. 2. Schematic of the opening delamination test apparatus.

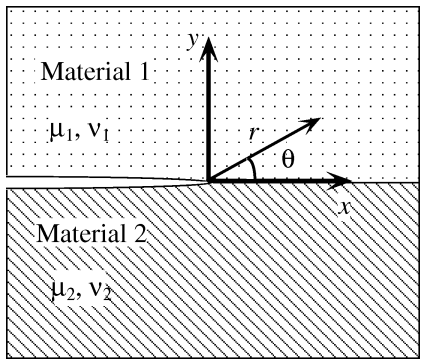


Fig. 3. Coordinate system around an interface crack tip.

it depends on the size and shape of the specimen. Thus, we used the stress intensity factors of an interface crack between dissimilar materials at the onset of delamination as delamination strength.

If a coordinate system around an interface crack is defined as shown in Fig. 3, the asymptotic solution of the stress components along the x-axis in the vicinity of an interface crack tip is expressed as [15]

$$(\sigma_{xy} + i\sigma_{xy})_{\theta=0} = \frac{K_{\mathrm{I}} + iK_{\mathrm{II}}}{\sqrt{2\pi r}} \left(\frac{r}{l_k}\right)^{i\varepsilon} \tag{1}$$

where K_{I} and K_{II} represent the stress intensity factors of the interface crack for Mode I and Mode II deformations, respectively, l_k is a characteristic length, which can be taken as an arbitrary constant, and ε is a bimaterial constant defined as

$$\varepsilon = \frac{1}{2\pi} \ln \left[\left(\frac{\kappa_1}{\mu_1} + \frac{1}{\mu_2} \right) \Big/ \left(\frac{\kappa_2}{\mu_2} + \frac{1}{\mu_1} \right) \right] \tag{2}$$

$$\kappa_i = \begin{Bmatrix} 3 - 4\nu_i & \text{Plane Strain} \\ (3 - \nu_i)/(1 + \nu_i) & \text{Plane Stress} \end{Bmatrix} \tag{3}$$

where (μ_1, μ_2) and (ν_1, ν_2) are the shear moduli and Poisson's ratios for materials 1 and 2, respectively. The characteristic

length l_k should be fixed at a certain value. Although Rice [16] recommended that l_k should be taken as the size of a fracture process zone, it is difficult to determine this size. In our previous study [17], we used $l_k = 10$ μm for convenience. When the value of l_k is changed to (l'_k), $K_{\rm I}$ and $K_{\rm II}$ are transformed into $K'_{\rm I}$ and $K'_{\rm II}$, as shown in [17]

$$\begin{pmatrix} K'_{\rm I} \\ K'_{\rm II} \end{pmatrix} = \begin{bmatrix} \cos Q & -\sin Q \\ \sin Q & \cos Q \end{bmatrix} \begin{pmatrix} K_{\rm I} \\ K_{\rm II} \end{pmatrix} \tag{4}$$

$$Q = \varepsilon \ln \left(\frac{l'_k}{l_k} \right). \tag{5}$$

We need to consider the sign of $K_{\rm II}$ for the interface crack because the deformation mode of the interface crack between dissimilar materials depends on the direction of shear stress around the crack tip. When the interface crack is located on the left side, and material indices 1 and 2 belong to $y \geq 0$ and $y < 0$, respectively, as shown in Fig. 3, we accept the sign of $K_{\rm II}$ in the case of $\varepsilon < 0$, but use the reverse sign of $K_{\rm II}$ in the case of $\varepsilon > 0$.

The total stress intensity factor K_i is defined as follows in order to take account of the effect of Mode I and Mode II simultaneously

$$K_i = \sqrt{K_{\rm I}^2 + K_{\rm II}^2}. \tag{6}$$

The energy release rate G for the interface crack is given in [18] as

$$G = \beta \left(K_{\rm I}^2 + K_{\rm II}^2 \right) \tag{7}$$

$$\beta = \frac{1}{16 \cosh^2(\varepsilon \pi)} \left(\frac{\kappa_1 + 1}{\mu_1} + \frac{\kappa_2 + 1}{\mu_2} \right). \tag{8}$$

It is determined from (6) and (7) that the total stress intensity factor K_i is related to the square root of the energy release rate G.

In our previous study [19], we evaluated the mixed mode fracture toughness of interfaces between the ACF and a Si chip/a substrate using mixed mode stress intensity factors between dissimilar materials. In this study, the targets of evaluation were interface cracks induced only by vapor pressure. It resulted in the fracture mode of cracks which were close to mode I. Therefore, K_i will be used instead of $K_{\rm I}$ and $K_{\rm II}$ to simplify the evaluation. Fortunately, K_i is independent of the size of l_k, and the size of l_k does not need to be considered in this study.

C. Estimation of Delamination Toughness

Three types of ACFs, ACF (A), ACF(B), and ACF(C), were used in the present study. The material properties are summarized in Table I. Table II shows the variation of Young's moduli with the test temperatures. In these properties, Young's moduli and the glass transition temperatures of ACFs were measured using a dynamic mechanical analyzer (DMA). Poisson's ratios of ACFs were substituted for by a common value of resin. All properties of the substrate were given by the supplier. The properties of the Si chip were the values of {111} faces obtained from the anisotropic stiffness [20]. The properties of Al were measured using an Instron-type testing machine (Shimazu Autograph 5000E). All the ACFs contained nickel(= Ni) particles of 3 μm in diameter as conductive particles, and the ACF(C) had two layers, the chip-side layer and the substrate-side layer as shown in Table I. The thicknesses of the two layers were almost the same, and both of them included the same Ni particles.

TABLE I
MATERIAL PROPERTIES AT ROOM TEMPERATURE

Material	E (GPa)	ν	T_g (°C)	CTE(10^{-6}/°C) <Tg	>Tg
ACF (A)	1.84	0.38	126	100	800
ACF (B)	2.52	0.38	160	100	400
ACF (C)-Chip	2.78	0.38	155	80	300
ACF (C)-Sub.	2.65	0.38	126	90	600
Substrate	16.5	0.20	156	11.6	1.4
Si chip	170	0.30		3	
Al	68.9	0.355		23	

E: Young's modulus, : Poisson's ratio, T_g: glass transition temperature, CTE: coefficient of thermal expansion, ACF (C)-Chip: Chip side of the ACF (C), ACF (C)-Sub.: Substrate side of the ACF (C).

TABLE II
VARIATION OF YOUNG'S MODULI (GPA) WITH TEST TEMPERATURE

	ACF (A)	ACF (B)	ACF (C)		Substrate
			Chip	Sub.	
60°C	1.18	1.87	2.21	1.32	16.3
95°C	1.02	1.61	1.97	1.08	15.7
120°C	0.76	1.42	1.71	0.82	15.3
240°C	0.02	0.06	0.12	0.03	5.13

As a measure of delamination strength, delamination toughness expressed by the stress intensity factors was calculated from the load at the onset of delamination, using the modified virtual crack extension method in conjunction with the two-dimensional thermoelastic finite-element method (FEM) [21]–[23]. This program was developed in our previous study [21], and it can provide the accurate stress intensity factors for an interface crack between dissimilar materials.

The effect of the residual stress was considered when determining the delamination toughness, using the stress-free temperature [19]. The stress-free temperature was determined using the curvature of the bimetal specimen as shown in Fig. 4. Usually, the first heating and first cooling show different curves for the curvature of the bimetal specimen. However, the first cooling and later cycles were almost identical in this case. We determined the stress-free temperature (T_f) when the curvature of the bimetal specimen shows 0 during the first cooling cycle.

Effective experimental delamination loads were not obtained for the lap joint specimens and the three-point bending specimens of the ACF(A) at room temperature, for all types of test specimens of the ACF(B) at room temperature, or for the lap joint specimens of the ACF(C) at room temperature, because no crack propagated along an interface between dissimilar materials, but rather propagated into the Si chip or the substrate. Only the opening delamination tests were performed for the Al pattern-ACF-substrate joints.

In the present study, we employed the total stress intensity factor, defined by (6), calculated from the maximum load of the delamination test. In all cases, the maximum load corresponded

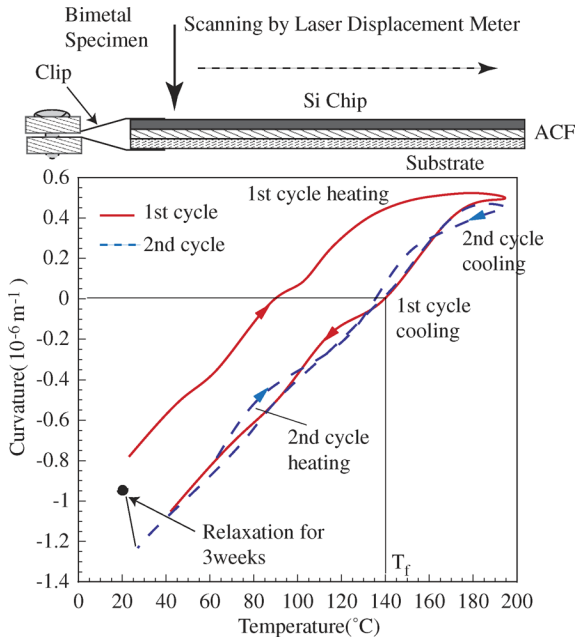


Fig. 4. Curvature of a bimetal specimen and the definition of stress free temperature T_f (Case of Adhesive A).

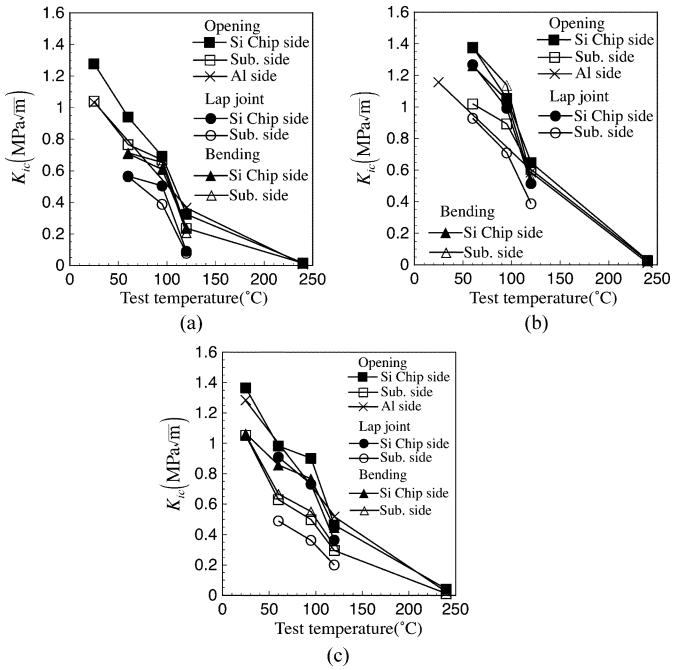


Fig. 5. Variation of delamination fracture toughness (the total stress intensity factor at the onset of delamination) with temperature (Si chip side: crack between the Si chip and ACF; Sub. side: crack between substrate and ACF; Al side: crack between Al and ACF). (a) ACF(A). (b) ACF(B). (c) ACF(C).

with the load at the onset of delamination. The calculation from the maximum load to the total stress intensity factors was carried out using the virtual crack extension method in conjunction with the FEM, which was developed in our previous study [21]. The variations of the delamination toughness with temperature are shown in Fig. 5. The values of the delamination toughness at 240 °C obtained from the opening delamination tests are

TABLE III
DELAMINATION TOUGHNESS OF OPENING DELAMINATION TEST AT 240 °C

	Interface	ACF(A)	ACF(B)	ACF(C)
K_{iC} (MPa$\sqrt{m}$)	Si chip side	0.0160	0.0297	0.0422
	Sub. side	0.0143	0.0260	0.0116
	Al side	0.0077	0.0130	0.0230

(Si chip side : A crack between Si chip and ACF, Sub. side : A crack between Substrate and ACF, Al side : A crack between Al and ACF. The underlined value indicates the minimum delamination toughness for each system).

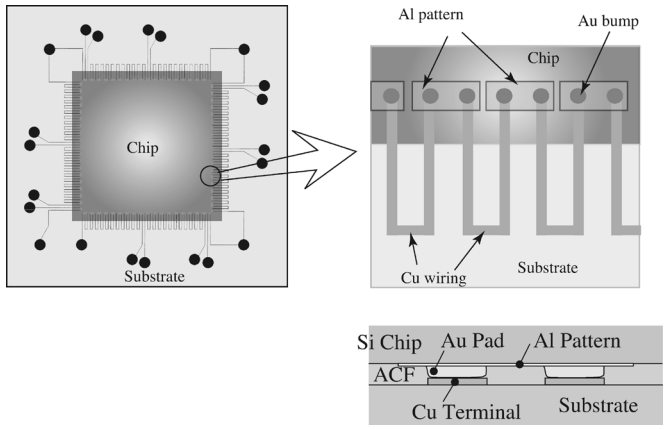


Fig. 6. Schematic of test flip chip for a conductive test.

shown in Table III. The delamination toughness decreased remarkably with the increase in temperature in all specimens. At 240 °C, ACF(A) and ACF(B) have the lowest delamination at the interface between the Al pattern and the ACF, while ACF(C) had its lowest delamination at the interface between the substrate and the ACF. These facts mean that the weakest part in the flip chip at the solder reflow temperature was the interface between the Al pattern and the ACF when ACF(A) and ACF(B) were used, and was the interface between the substrate and the ACF when ACF(C) was used. The delamination toughness of ACF(C) strongly depended on the side on which the initial delamination was introduced, because ACF(C) is composed of two layers with different Young's moduli and different coefficients of linear expansion.

III. MOISTURE/REFLOW SENSITIVITY TEST FOR FLIP CHIP USING THE ACF

Electrical conduction tests were carried out to estimate the failure of a test flip chip using ACF shown in Fig. 6 during the solder reflow process after moisture absorption, which is called the moisture/reflow sensitivity test hereafter. The failure of the test flip chip was detected by measuring the electric resistance of a daisy-chain circuit connecting all the gold (Au) bumps and copper (Cu) terminals in the test flip chip, as shown in Fig. 6. Electrical disconnection was assumed to be caused by a mechanical failure. The Cu terminals were plated with Ni and Au. The test flip chip had 184 bumps with a pitch of 200 μm, a substrate with a thickness of 0.8 mm and Cu terminals with a thickness of 20 μm on the substrate.

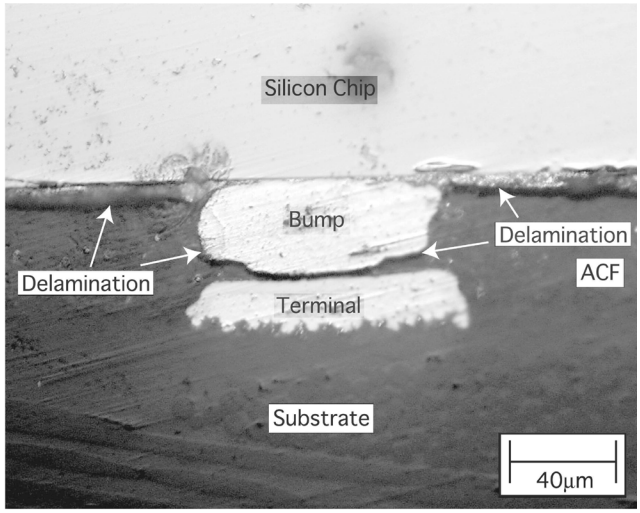
TABLE IV
NUMBER OF DISCONNECTED FLIP CHIPS AFTER MOISTURE/REFLOW SENSITIVITY TEST

System	Disconnected Chips		
	RF1	RF2	RF3
ACF(A)	10/10	–	–
ACF(B)	2/10	2/10	2/10
ACF(C)	7/10	7/10	7/10

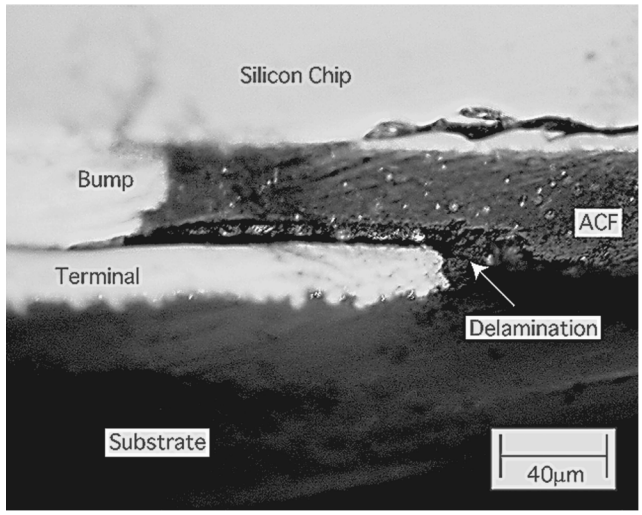
(Disconnected Chips/Number of test specimens)
RF1, RF2, RF3: First, second and third reflow processes.

First the test flip chip was baked at 125 °C for 24 h, then exposed to an atmosphere of 85 °C/85%RH (= relative humidity) for 168 h, during which moisture absorption was measured with a balance, and it was finally heated in a thermostatic oven at 240 °C for 40 s to simulate the solder reflow process. After the heating process, the electric resistance of a daisy-chain circuit on the test flip chip was measured to detect any disconnection of the ACF interconnections. All disconnected specimens showed infinitely large resistance.

Table IV shows the number of disconnected test flip chips after the moisture/reflow sensitivity tests. Obviously ACF(B) showed the highest durability against the moisture/reflow sensitivity tests, and ACF(A) showed the lowest durability. These findings are related to the facts that ACF(B) had the highest minimum-delamination toughness and that ACF(A) had the lowest minimum-delamination toughness, as shown in Table IV. The test flip chips that did not fail during the first heating process did not fail in the second and third heating processes either. It is expected that the vapor pressure during the solder reflow process caused the disconnection of the ACF interconnection. The test flip chip was dried during the first heating process, and the vapor pressures during the second and third heating processes were supposed to be less than that during the first heating process. So failure could have occurred only in the first heating process. Fig. 7 shows the microphotographs of the test flip chips after moisture/reflow sensitivity tests for ACF(A) and ACF(C). The delamination was observed at the interface between the Au bump/Al pattern and the ACF for ACF(A). In the case of ACF(C), the delamination occurred at the interface between the Cu terminal/substrate and the ACF. Such delamination causes electrical disconnection.



(a)



(b)

Fig. 7. Microphotograph of test flip chip after moisture/reflow sensitivity test. (a) ACF(A). (b) ACF(C).

IV. ESTIMATION OF DELAMINATION IN THE FLIP CHIP DURING THE SOLDER REFLOW PROCESS

A. Estimation of Vapor Pressure in Flip Chip During Solder Reflow Process

The diffusion coefficients and Henry's law coefficients of the ACF and the substrate were determined for a diffusion analysis of the moisture absorption of the test flip chip, the results of which were utilized to calculate the vapor pressure in the test flip chip during the solder reflow process. Rectangular thin plate specimens of the ACF and the substrate were employed for this purpose, because one-dimensional (1–D) diffusion along the plate thickness can be assumed. The Henry's law coefficients of the ACF and the substrate were calculated with the following equation, using a saturated moisture concentration:

$$C(x, t = \infty) = \rho \times H \times p_{sv} \tag{9}$$

where C is the moisture concentration, ρ is the relative humidity, H is Henry's law coefficient, and P_{sv} is the saturated vapor pressure. The diffusion coefficients of the ACF and the substrate were determined by comparing the curve of experimentally determined weight gain of the test specimen versus time with the solution of the 1-D diffusion equation given by [24]

$$C(x,t) = N_S \left\{ 1 - \frac{4}{\pi} \sum_{k=1}^{\infty} \frac{1}{2k+1} \exp\left(-\frac{(2k+1)^2 \pi^2}{4L^2} Dt \right) \times \sin \frac{(2k+1)\pi x}{2L} \right\} \tag{10}$$

where D is the diffusion coefficient, Ns is the saturated moisture concentration, x is the distance of the 1-D diffusion direction, and L is the thickness of the specimen. The Henry's law coefficients and diffusion coefficients of the ACFs and the

TABLE V
HENRY'S LAW COEFFICIENTS AND DIFFUSION COEFFICIENTS OF ACFS AND SUBSTRATE

Condition (°C/%RH)	Material	H (mg/mm^{3}MPa)	D (10^{-2}mm^2/hr)
30°C/80%RH	ACF (A)	3.050	0.552
	ACF (B)	4.545	0.402
	ACF (C)	3.120	0.480
(*40°C/80%RH)	Substrate	1.508*	0.080*
85°C/85%RH	ACF (A)	0.5204	5.70
	ACF (B)	0.6951	3.36
	ACF (C)	0.5405	4.50
	Substrate	0.194	0.75
120°C/100%RH	ACF (A)	0.233	9.72
	ACF (B)	0.2993	5.76
	ACF (C)	0.2326	8.64
	Substrate	0.0808	2.25

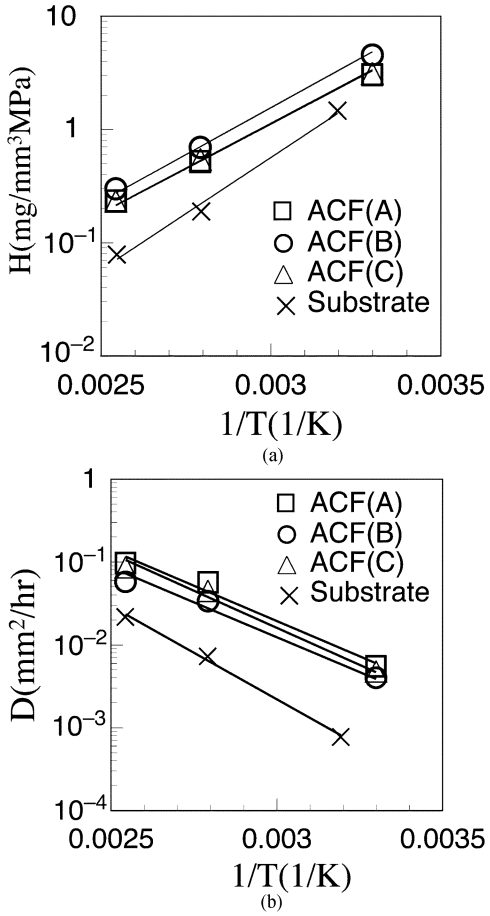


Fig. 8. Arrehnius plots of Henry's law coefficient and diffusion coefficient. (a) Henry's law coefficient. (b) Diffusion coefficient.

substrate obtained by the above-mentioned method are summarized in Table V for several environmental conditions. Arrehnius plots of Henry's law coefficient H and the diffusion coefficient D are shown in Fig. 8. The following equations were fitted to

TABLE VI
VARIATION OF ACTIVATION ENERGIES AND PRE-EXPONENTIAL FACTORS

	ACF (A)	ACF (B)	ACF (C)	Substrate
D_0(10^3mm^3/hr)	2.47	1.42	3.80	12.7
E_D(10^4J/mol)	3.257	3.228	3.429	4.304
H_0(10^{-6}mg/mm^3/MPa)	20.68	16.92	19.89	0.67
E_H(10^4J/mol)	–3.019	–3.167	–3.036	–3.792

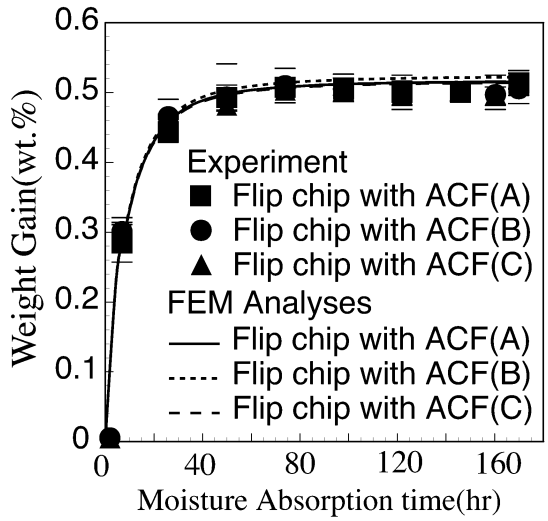


Fig. 9. Weight gains of test flip chips with moisture absorption time.

the obtained coefficients using the least square approximation as shown in Fig. 8:

$$\left.\begin{aligned} D &= D_0 \exp\left(\tfrac{-E_D}{RT}\right) \\ H &= H_0 \exp\left(\tfrac{-E_H}{RT}\right) \end{aligned}\right\} \tag{11}$$

where D_0 and H_0 are empirical constants, E_D and E_H are the activation energies, R is the universal gas constant (8.314 J/mol · K), and T is the absolute temperature (K). The pre-exponential factors and activation energies of the respective materials are shown in Table VI.

Three-dimensional (3–D) diffusion analyses of the test flip chips were performed using a finite element computer code (MARC) to obtain the moisture concentration of the test flip chip package. The temperature and the relative humidity around the test flip chip were 85 °C and 85%RH, respectively. The weight gains obtained from the 3-D diffusion analyses agreed well with those obtained from the moisture absorption tests, as shown in Fig. 9, and the reliability of the 3-D diffusion analyses was verified. The figure shows that the test flip chips reached a saturated moisture absorption condition after three days. No large difference was found among the test flip chips interconnected by the ACF(A), ACF(B), and ACF(C). This is because almost all of the moisture was stored in the substrate, because the substrate had a very large volume compared with the ACF. As mentioned below, the failure of the test flip chip was induced by the vaporization of the moisture absorbed in the ACF. It should be noted that the durability of the flip chip interconnected by the ACF against the moisture/reflow sensitivity

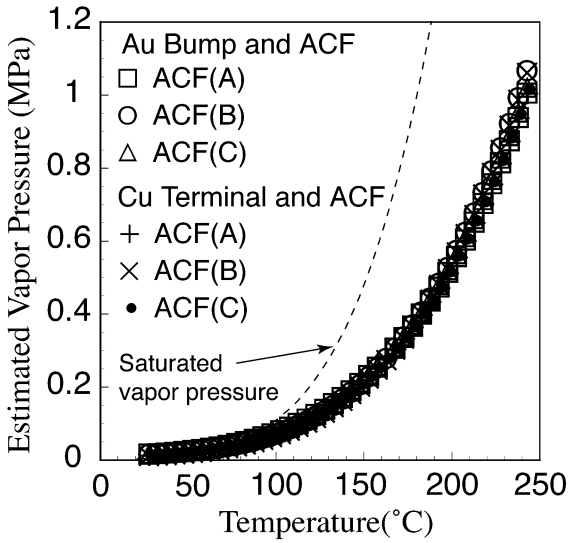


Fig. 10. Expected vapor pressure in test flip chip during the reflow process.

test was affected by the moisture absorption characteristics of the ACF.

A fine gap such as delamination or a crack was assumed to exist at the interface between the ACF and the Au bump or the Cu terminal. Then an equilibrium condition expressed by Henry's law could be assumed to hold between the vapor pressure in the gap and the moisture concentration in the ACF. The vapor pressure in the gap during the solder reflow process was predicted from Henry's law as

$$\left.\begin{array}{ll} P_V = P_{\mathrm{SV}} & (C_{\max} \geq HP_{\mathrm{SV}} \text{ at } T_R{}^{\circ}\mathrm{C}) \\ P_V = \frac{C_{\max}}{H} & (C_{\max} < HP_{\mathrm{SV}} \text{ at } T_R{}^{\circ}\mathrm{C}) \end{array}\right\} \quad (12)$$

where $C_{\max}$ is the maximum moisture concentration, $T_R{}^{\circ}$C is the reflow temperature, P_{SV} is the saturated vapor pressure, and P_V is the predicted vapor pressure in the gap. Fig. 10 shows the predicted vapor pressure during the solder reflow process in the gap between the ACF and the Au bump or the Cu terminal located at the corner of the test flip chip, at which the moisture concentration was at its maximum in the diffusion analysis.

B. Estimation of Delamination of the Flip Chip During Solder Reflow Process

At the solder reflow temperature of 240 °C, a small compressive stress or tensile stress was expected to act on the ACF layer between the Au bump and the Cu terminal. It is also reasonable to consider that the interface between the ACF and the bump or the terminal could be delaminated even by a small amount of vapor pressure at the reflow temperature, because the adhesive strength between the epoxy resin, the matrix resin of the ACFs, and the gold, the noble metal used for the bumps and plating on the Cu terminals, was very small. Accordingly we assumed that the interface between the ACF and the Au bump or the Cu terminal was completely delaminated when estimating the delamination of the test flip chip during the solder reflow process. The vapor pressure acted on the gap generated by the delamination between the ACF and the bump or the terminal. We considered a penny-shaped crack with the same size as the Au bump or the Cu terminal at the interface between the ACF and the Si chip, the ACF and the Al pattern, or the ACF and the substrate, as shown in Fig. 11.

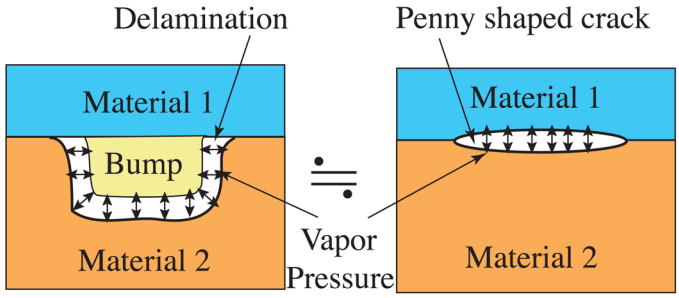


Fig. 11. Assumption of penny-shaped crack used in this study.

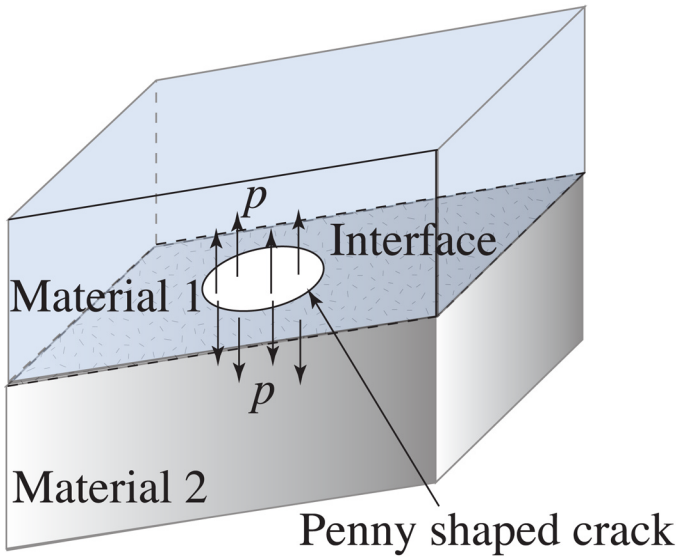


Fig. 12. Penny-shaped crack between dissimilar materials.

Furthermore, to predict the crack propagation caused by the vapor pressure, we used the stress intensity factors of a penny-shaped crack between dissimilar materials subjected to uniform tension applied to its crack surface, as shown in Fig. 12. The stress intensity factors K_I and K_{II} were given by Kassir and Bregman [25], as follows:

$$K_I + iK_{II} = 2pa\sqrt{a}\frac{\Gamma(2+\gamma)}{\Gamma(0.5+\gamma)} \quad (13)$$

where p is the uniform tension applied to the crack surface, a is the radius of a penny-shaped crack, $\Gamma(x)$ is the gamma function, and $i = \sqrt{-1}$. The bielastic constant γ is given in terms of the shear moduli μ_i and Poisson's ratios ν_i $(i = 1,2)$ of the materials 1 and 2 by

$$\gamma = \frac{1}{2\pi i}\ln\left(\frac{\mu_2 + \mu_1(3-4\nu_2)}{\mu_1 + \mu_2(3-4\nu_1)}\right). \quad (14)$$

We calculated the stress intensity factors of a penny-shaped crack at the interface between the ACF and the Si chip (or the Al pattern or the substrate) from (13) and (14) when vapor pressure was applied to the crack surface. In this case, the penny-shaped

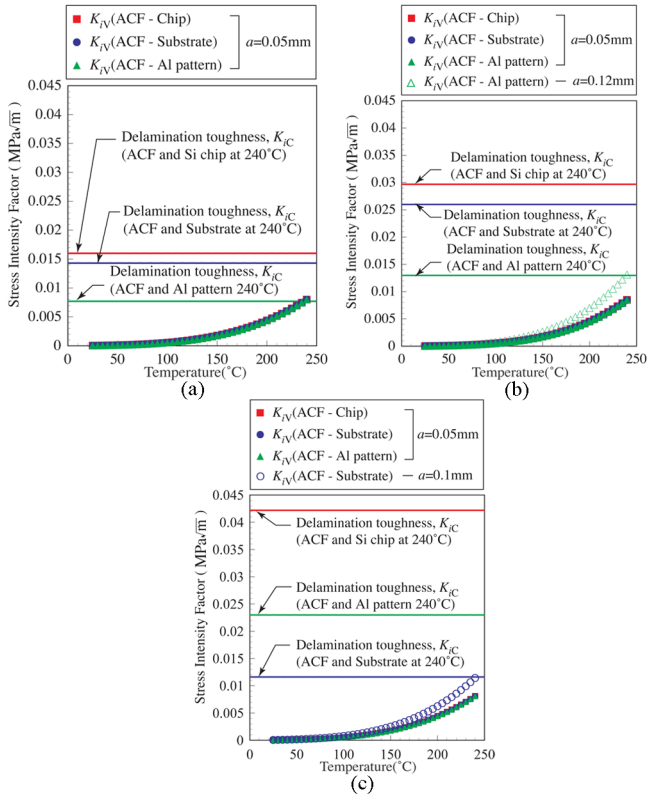


Fig. 13. Comparison between the delamination toughness and the stress intensity factors during the reflow process after the moisture absorption test (K_{iV}; Total stress intensity factors caused by vapor pressure in a penny-shaped crack, K_{iC}; Delamination toughness measured by delamination test at 240 °C). (a) ACF(A). (b) ACF(B). (c) ACF(C).

crack was the same size ($a = 50$ μm) as the gold bump and the Cu terminal. Fig. 13 shows the comparison between the stress intensity factor (K_{iV}) caused by the predicted vapor pressure during the solder reflow process and the delamination toughness (K_{ic}) measured by the delamination test using the opening delamination specimen at 240 °C. It is found from the figure that the values of the stress intensity factor K_{iV} are almost the same for any combinations of materials 1 and 2.

The results of ACF(A) show that the stress intensity factors of the interface crack between the ACF and the Si chip and between the ACF and the substrate caused by the vapor pressure during the solder reflow process were lower than the delamination toughness at 240 °C. On the other hand, the stress intensity factor of the interface crack between the ACF and the Al pattern caused by the vapor pressure was slightly higher than the delamination toughness at 240 °C. Consequently, the delamination in the test flip chip interconnected by ACF(A) was expected to propagate along the interface between the ACF and the Al pattern from the bottom of the Au bump due to the vapor pressure during the solder reflow process after moisture absorption. Once the interface between the ACF and the Al pattern was delaminated, the delamination propagated along the interface between the ACF and the Si chip until the vapor pressure was released from the test flip chip.

In the case of system B interconnected by ACF(B), the values of the delamination toughness for all the jointed interfaces were higher than the stress intensity factors caused by the vapor pressure during the reflow process. So, it is likely that ACF(B) was not delaminated. In other words, an initial delamination larger than the bump radius is required for the propagation of the delamination. If we assume that system B had a penny-shaped crack with a radius of 120 μm at the interface between the ACF and the Al pattern, the total stress intensity factor due to the vapor pressure was almost the same as the delamination toughness of the interface crack between the ACF and the Al pattern. Therefore, we could presume that the disconnected test flip chips of the system B shown in Table IV had a delamination or void equivalent to a penny-shaped crack with a radius of 120 μm at the interface between the ACF and the Al pattern. Similarly, if we presume that the test flip chip of ACF(C) had a penny-shaped crack with a radius of 100 μm at the interface between the ACF and the substrate around the copper terminal, the delamination condition would be satisfied. The results predicted by the quantitative estimation method presented in this study can explain the results of the moisture/reflow sensitivity tests shown in Table IV.

V. Conclusion

To estimate the moisture/reflow delamination of a flip chip interconnected by an ACF, we performed moisture/reflow sensitivity tests on test flip chips, conducted moisture diffusion analyses, and performed tests to measure the delamination toughness of ACF joints. The conclusions of the present study are as follows.

1) We can evaluate the delamination strength of ACF joints by using the delamination toughness defined by the total stress intensity factor of an interface crack between dissimilar materials at the onset of delamination. Such delamination toughness can be utilized in the practical design of electronic packaging.
2) We can estimate the vapor pressure of a flip chip during the solder reflow process after moisture absorption by a moisture diffusion analysis of the flip chip.
3) The moisture/reflow sensitivity tests of test flip chips show that a large scale of delamination occurs, resulting in electric disconnection, when the stress intensity factor caused by the vapor pressure during the reflow process after moisture absorption exceeds the fracture toughness of the ACF joint. Such a method can be applied to prevent the delamination of ACF joints in electronic packaging.
4) The ACF is a viscoelastic material around T_g, and is a viscoplastic material at high temperatures. However, in this study we only took account of the temperature dependence of the elastic properties of the ACF because the heating rate is very high in the case of the solder reflow process, and it is kept at the reflow temperature for only 40 s. In this short period, the deformation is dominated relatively more by elasticity than viscosity. Moreover, the ACF layer is very thin, and this layer is constrained by the Si chip and the substrate. Therefore, the effect of viscosity is relatively small on the opening of a crack by vapor pressure. If we consider the shear deformation of the ACF due to thermal stress, the viscosity of the ACF must be taken into account.

REFERENCES

[1] H. Kristiansen and J. Liu, "Overview of conductive adhesive interconnection technologies for LCDs," *IEEE Trans. Comp., Packag., Manufact. Technol. A*, vol. 21, no. 2, pp. 208–214, Jun. 1998.

[2] M. J. Yim and K. W. Paik, "Design and understanding of anisotropic conductive films (ACFs) for LCD packaging," *IEEE Trans. Comp. , Packag., Manufact. Technol. A*, vol. 21, no. 2, pp. 226–234, Jun. 1998.

[3] K. Suzuki, O. Suzuki, and M. Komagata, "Conductive adhesive materials for lead solder replacement," *IEEE Trans. Comp., Packag., Manufact. Technol. A*, vol. 21, no. 2, pp. 252–258, Jun. 1998.

[4] J. C. Jagt, "Reliability of electrically conductive adhesive joints for surface mount applications; a summary of the state of art," *IEEE Trans. Comp., Packag., Manufact. Technol. A*, vol. 21, no. 2, pp. 215–225, Jun. 1998.

[5] U. Behner, R. Haug, R. Schütz, and H. Hartnagel, "Characteriztion of anisotropically conductive adhesive interconnections by $1/f$ noise measurement," *IEEE Trans. Comp., Packag., Manufact. Technol. A*, vol. 21, no. 2, pp. 243–247, Jun. 1998.

[6] G. Reza, "Chip scale package issues," *Microelectron. Rel.*, vol. 40, pp. 1157–1161, 2000.

[7] Y. W. Chiu, Y. C. Chan, and S. M. Lui, "Study of short-circuiting between adjacent joints under electric effects in fine pitch anisotropic conductive adhesive interconnects," *Microelectron. Rel.*, vol. 42, pp. 1945–1951, 2002.

[8] M. Teo, S. G. Mhaisalkar, E. H. Wong, P. S. Teo, C. C. Wong, K. Ong, C. F. Goh, and L. K. Teh, "Correlation of material properties to reliability performance of anisotropic conductive adhesive flip chip packages," *IEEE Trans. Comp., Packag., Manufact. Technol. A*, vol. 28, no. 1, pp. 157–164, Mar. 2005.

[9] C. Y. Yin, M. O. Alam, T. C. Chan, C. Bailey, and H. Lu, "The effect of reflow process on the contact resistance and reliability of anisotropic conductive film interconnection for flip chip on flex applications," *Microelectron. Rel.*, vol. 43, pp. 625–633, 2003.

[10] A. Seppala and E. Ristolainen, "Study of adhesive flip chip bonding process and failure mechanism of ACA joints," *Microelectron. Rel.*, vol. 44, pp. 639–648, 2004.

[11] T. Hattori, S. Sakata, and G. Murakami, "A stress singularity parameter approach for evaluating the interfacial reliability of plastic encapsulated LSI devices," *ASME J. Electron. Packag.*, vol. 111, pp. 243–245, 1989.

[12] T. Ikeda, I. Arase, Y. Ueno, and N. Miyazaki, "Strength evaluation of electronic plastic packaging using stress intensity factors of V-notch," *Comput. Model. Simul. Eng.*, vol. 1, pp. 91–97, 2000.

[13] T. Ikeda, I. Arase, Y. Ueno, N. Miyazaki, N. Ito, M. Nakatake, and M. Sato, "Strength evaluation of plastic packages under solder reflow process using stress intensity factors of V-notch," *J. Electron. Packag.*, vol. 125, pp. 31–38, 2003.

[14] G. W. Kim and K. Y. Lee, "Improving the reliability of a plastic IC package in the reflow soldering process by DOE," *Solder. Surf. Mount Technol.*, pp. 40–48, 2005.

[15] F. Erdogan, "Stress distribution in a nonhomogeneous elastic plan with crack," *J. Appl. Mech.*, vol. 30, pp. 232–236, 1963.

[16] J. R. Rice, "Elastic fracture mechanics concepts for interfacial crack," *J. Appl. Mech.*, vol. 55, pp. 98–103, 1988.

[17] T. Ikeda, N. Miyazaki, and T. Soda, "Mixed mode fracture criteria of interface crack between dissimilar materials," *Eng. Fracture Mech.*, vol. 45, pp. 725–735, 1998.

[18] B. Malyshev and R. Salganik, "The strength of adhesive joints using the theory of cracks," *Int. J. Fract. Mech.*, vol. 1, pp. 114–119, 1965.

[19] W. K. Kim, T. Ikeda, and N. Miazaki, "Reliability evaluation of flip chip using stress intensity factors of an interface crack," in *Proc. InterPACK03*, 2003, pp. 1–7.

[20] INSPEC, Properties of Silicon, EMIS Data Reviews Series, no. 4, p. 14, 1988.

[21] T. Ikeda and C. T. Sun, "Stress intensity factor analysis for an interface crack between dissimilar isotropic materials under thermal stress," *Int. J. Fract.*, vol. 111, pp. 229–249, 2001.

[22] N. Miyazaki, T. Ikeda, T. Soda, and T. Munakata, "Stress intensity factor analysis of interface crack using boundary element method (Application of virtual crack extension method)," *JSME Int. J.*, vol. 36, pp. 36–42, 1993.

[23] ——, "Stress intensity factor analysis of interface crack using boundary element method—application of contour-integral method," *Eng. Fract. Mech.*, vol. 45, pp. 599–610, 1993.

[24] M. Houzawa, M. Toda, K. Kikuchi, T. Yonemoto, and T. Tsukada, *Creative Chemical Engineering Course 6, Diffusion and Transport Phenomena*. Tokyo, Japan: Baifu-kan, 1996.

[25] M. K. Kassir and A. M. Bregman, "The stress intensity factors for penny shaped crack between two dissimilar materials," *J. Appl. Mech.*, vol. 39, pp. 308–310, 1972.

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